Amendments to the Specification:

Delete paragraph [0015].

Amend the paragraph numbered [0028] to read as follows:

A first display device according to the present invention is characterized by comprising a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal; an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit; horizontal video start position detection means for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value; horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a second threshold value; calculation means for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position; judgment means for judging whether or not the result of the calculation by the calculation means coincides with a required reference value; frequency control value adjustment means for calculating, when it is judged that the result of the calculation by the calculation means and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation means, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and threshold value control means for controlling, for each vertical period, [[a]] the second threshold

A1 cont

a1 cmdd

value depending on the level of the video data ~~outputted from the analog-to-digital converter~~ at the horizontal video end position detected ~~with~~ WITHIN the vertical period.

Amend paragraph numbered [0030] to read as follows:

A second display device according to the present invention is characterized by comprising a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal; an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit; a horizontal video start position detection circuit for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value; a horizontal video end position detection circuit for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on the basis of a second threshold value; a calculation circuit for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position; a judgment circuit for judging whether or not the result of the calculation by the calculation means coincides with a required reference value; a frequency control value adjustment circuit for calculating, when it is judged that the result of the calculation by the calculation circuit and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation circuit, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit; and a threshold value control circuit

a2 cont

for controlling, for each vertical period, [[a]] the second threshold value depending on the level of the video data ~~outputted from the analog-to-digital converter~~ at the horizontal video end position detected within the vertical period.

Amend the paragraph numbered [0032] to read as follows:

A first pixel corresponding display device according to the present invention is characterized by comprising a clock generation circuit for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal; an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit; detection means for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines; calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position farthest from the horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field; frequency adjustment means for controlling the clock generation circuit on the basis of the result of the calculation by the calculation means, to adjust the frequency of the sampling clocks; judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the

result of the calculation by the calculation means; and means for stopping, ~~when it is judged that~~ while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

Amend the paragraph numbered [0033] to read as follows:

A second pixel corresponding display device according to the present invention is characterized by comprising a clock generation circuit for generating sampling clocks on the basis of a horizontal synchronizing signal of an input video signal; an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit; a detection circuit for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines; a calculation circuit for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position farthest from a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video end positions detected within one field, the number of sampling clocks corresponding to the distance between the horizontal video start position and the horizontal video end position of the input video signal for the field; a frequency adjustment circuit for controlling the clock generation circuit on the basis of the result of the calculation by the calculation circuit, to adjust the frequency of the sampling clocks; a judgment circuit for judging for each field whether or not the

width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation circuit; and a circuit for stopping, ~~when it is judged that~~ while the width of the region where the input video exists is being judged to be smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field.

Amend the paragraph numbered [0070] to read as follows:

When the result of the subtraction does not coincide with "1024" [[or]] nor "1025", a coincidence/non-coincidence judgment signal is brought into an L level. When the result of the subtraction coincides with ~~both~~ either "1024" [[and]] or "1025", the coincidence/non-coincidence judgment signal is brought into an H level.

Amend the paragraph numbered [0089] to read as follows:

In FIGS. 4 and 5, a signal (a) indicates an ideal analog input video signal which is not dull. A signal (b) or a signal (c) indicates an actual analog input video signal which is dull. ~~As indicated by the signal (b) or (c),~~ This example shows a case where the dullness appears more significantly at the time of the fall than that at the time of the rise as indicated by the signal (b) or (c). THs and THe respectively indicate a threshold value for start position judgment and a threshold value for end position judgment

Amend the paragraph numbered [0119] to read as follows:

The field integration averaging circuit 86 calculates for each filed the average of output values of the absolute value circuit 85 in order to increase[[s]] the reliability of the result of the output of the absolute value circuit 85, ~~and calculates for each field the average of output values of the absolute value circuit 85 in order to~~ and prevent an erroneous operation from being immediately performed by noises or the like. That is, the average of the output values ~~for horizontal lines which are~~ outputted from the absolute value circuit 85 ~~in one field are added, and the result of the addition is divided by the number of horizontal lines~~ is found, thereby calculating the average of the output values of the absolute value circuit 85 per field.

a7